POWER SEMICONDUCTOR DEVICES AND METHODS OF MANUFACTURE

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims the benefit of the following provisionally-filed U.S. patent application:

No. 60/533,790, entitled "Power Semiconductor Devices and Methods of Manufacture," by Ashok et al. filed Dec. 30, 2003.

This application is a continuation-in-part of the following commonly-assigned U.S. patent applications:

Ser. No. 10/640,742, entitled "Improved MOS Gating Method for Reduced Miller Capacitance and Switching Losses," by Kocon et al., filed Aug. 14, 2003; now U.S. Pat. No. 6,870,220;

Ser. No. 10/442,670, entitled "Structure and Method for Forming a Trench MOSFET Having Self-Aligned Features," by Herrick, filed May 20, 2003 now U.S. Pat. No. 6,916,745.

This application is related to the following commonly-assigned U.S. patent applications:

Ser. No. 10/155,554, entitled "Field Effect Transistor and Methods of its Manufacture," by Mo et al., filed May 24, 2002;

Ser. No. 10,209,110, entitled "Dual Trench Power MOSFET," by Sapp, filed Jul. 30, 2002;

Ser. No. 09/981,583, entitled "Semiconductor Structure with Improved Smaller Forward Loss and Higher Blocking Capability," by Kocon, filed Oct. 17, 2001;

Ser. No. 09/774,780, entitled "Field Effect Transistor Having a Lateral Depletion Structure," by Marchant, filed Jan. 30, 2001;

Ser. No. 10/200,056, entitled "Vertical Charge Control Semiconductor Device with Low Output Capacitance," by Sapp et al., filed Jul. 18, 2002;

Ser. No. 10/288,982, entitled "Drift Region Higher Blocking Lower Forward Voltage Drop Semiconductor Structure," by Kocon et al., filed Nov. 5, 2002;

Ser. No. 10/315,719, entitled "Method of Isolating the Current Sense on Planar or Trench Stripe Power Devices while Maintaining a Continuous Stripe Cell," by Yedinak, filed Dec. 10, 2002;

Ser. No. 10/222,481, entitled "Method and Circuit for Reducing Losses in DC-DC Converters," by Elbanhawy, filed Aug. 16, 2002;

Ser. No. 10/235,249, entitled "Unmolded Package for a Semiconductor Device," by Joshi, filed Sep. 4, 2002; and

Ser. No. 10/607,633, entitled "Flip Chip in Leaded Molded Package and Method of Manufacture Thereof," by Joshi et al., filed Jun. 27, 2003;

All of the above-listed applications are hereby incorporated by reference in their entirety.

BACKGROUND OF THE INVENTION

The present invention relates in general to semiconductor devices and in particular to various embodiments for improved power semiconductor devices such as transistors and diodes, and their methods of manufacture, including packages and circuitry incorporating the same.

The key component in power electronic applications is the solid state switch. From ignition control in automotive applications to battery-operated consumer electronic devices, to power converters in industrial applications, there is a need for a power switch that optimally meets the demands of the particular application. Solid state switches including, for example, the power metal-oxide-semiconductor field effect transistor (power MOSFET), the insulated-gate bipolar transistor (IGBT) and various types of thyristors have continued to evolve to meet this demand. In the case of the power MOSFET, for example, double-diffused structures (DMOS) with lateral channel (e.g., U.S. Pat. No. 4,682,405 to Blanchard et al.), trenched gate structures (e.g., U.S. Pat. No. 6,429,481 to Mo et al.), and various techniques for charge balancing in the transistor drift region (e.g., U.S. Pat. No. 4,941,026 to Temple, U.S. Pat. No. 5,216,275 to Chen, and U.S. Pat. No. 6,081,009 to Neilson) have been developed, among many other technologies, to address the differing and often competing performance requirements.

Some of the defining performance characteristics for the power switch are its on-resistance, breakdown voltage and switching speed. Depending on the requirements of a particular application, a different emphasis is placed on each of these performance criteria. For example, for power applications greater than about 300-400 volts, the IGBT exhibits an inherently lower on-resistance as compared to the power MOSFET, but its switching speed is lower due to its slower turn off characteristics. Therefore, for applications greater than 400 volts with low switching frequencies requiring low on-resistance, the IGBT is the preferred switch while the power MOSFET is often the device of choice for relatively higher frequency applications. If the frequency requirements of a given application dictate the type of switch that is used, the voltage requirements determine the structural makeup of the particular switch. For example, in the case of the power MOSFET, because of the proportional relationship between the drain-to-source on-resistance R_{DSon} and the breakdown voltage, improving the voltage performance of the transistor while maintaining a low R_{DSon} poses a challenge. Various charge balancing structures in the transistor drift region have been developed to address this challenge with differing degrees of success.

Device performance parameters are also impacted by the fabrication process and the packaging of the die. Attempts have been made to address some of these challenges by developing a variety of improved processing and packaging techniques.

Whether it is in ultra-portable consumer electronic devices or routers and hubs in communication systems, the varieties of applications for the power switch continue to grow with the expansion of the electronic industry. The power switch therefore remains a semiconductor device with high development potential.

BRIEF SUMMARY OF THE INVENTION

The present invention provides various embodiments for power devices, as well as their methods of manufacture, packaging, and circuitry incorporating the same for a wide variety of power electronic applications. Broadly, one aspect of the invention combines a number of charge balancing techniques and other techniques for reducing parasitic capacitance to arrive at various embodiments for power devices with improved voltage performance, higher switching speed, and lower on-resistance. Another aspect of the invention provides improved termination structures for low, medium and high voltage devices. Improved methods of fabrication for power devices are provided according to other aspects of the invention. Improvements to specific processing steps, such as formation of trenches, formation of dielectric layers inside trenches, formation of mesa structures, processes for reducing substrate thickness, among